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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,228	02/15/2002	Patrick J. Smith	TI-30704	2620

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	3

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,228	SMITH, PATRICK J.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "**said close portion**" in line 17. There is insufficient antecedent basis for this limitation in the claim. Also, "**aid**" in line 20 should be changed to "**said**".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buktenica et al. (5,669,009) (hereinafter Buktenica) in view of Hofmann et al. (6,513,089) (hereinafter Hofmann).

As to claim 1, Buktenica teaches a multiprocessor system comprising: a plurality of data processors (processing node 20), each data processor including: a data processing core (processor 11) capable of data processing according to program control and memory access, a memory forming a local portion of a unified memory (dual port memory 14) shared among said plurality of data processors, and a global memory arbitration logic (bus controller 16) connected to said data processing core and said memory of each of said data processors (Fig. 1 and col. 2, lines 37-59), said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor and a far connection to said data processing core of additional data processors (col. 5, lines 5-14 wherein requests from multiple processing nodes 20 are recognized on the basis of position on the global bus 18, and thus for every processing node there are always close and far connections with respect the plurality of processing nodes), said global memory arbitration logic arbitrating access to said unified memory granting a first type access among the data processing cores (e.g. read type via buses 15 and 20) and a second type access different from aid first type access among far data processing cores (e.g. write type via bus 18) (Figs. 1, 3, and col. 4, lines 39-65). However, Buktenica does not explicitly disclose granting a first type access to close data processing cores and a second type access to far data processing cores. Hofmann teaches high priority device is granted a read request while the write bus may be granted to another lower priority device with higher priority write request (abstract and col. 3, lines 10-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

implement different priority levels for reads and writes as taught by Hofmann for the close and fare processing cores in the system of Buktenica wherein the first type access (read) is granted to a high priority processing core and a second type access (write) is granted to another processing cores to allow processing cores with high demand for reads and writes to have more frequent accesses to the memory and to allow reads and writes to remain operational by a low priority processing core when the higher priority processing cores requests the corresponding other bus operation (col. 3, lines 10-19).

As to claim 2, Buktenica further teaches said local portion of said unified memory of each data processor is a dual port memory having a first port and a second port (memory 14) (Fig. 1 and col. 2, lines 46-59); and said global memory arbitration logic arbitrating access to said first port of said dual port memory among said close data processing cores thereby providing said first type access and arbitrating access to said second port of said dual port memory among said far data processing cores thereby providing said second type access (col. 4, lines 50-65).

As to claim 4, Buktenica further teaches each of said data processors further includes a peripheral bus (bus 18 and/or bus 20, bus 15) connected to said dual port memory for read and write access (Fig. 1), and Hofmann further teaches granting read access requests on said peripheral bus highest priority access to said first port and granting write access request on said peripheral bus highest priority access to said second port (col. 3, lines 10-19).

As to claim 5, Buktenica further teaches each of said data processors further includes a local memory (local memory 12) connected to said data processing core and

directly accessible by said data processing core and not directly accessible by data processing cores of other data processors (Fig. 1).

As to claim 6, Buktenica teaches a multiprocessor system comprising: a plurality of data processors (processing node 20), each data processor including: a data processing core (processor 11) capable of data processing according to program control and memory access, a memory forming a local portion of a unified memory (dual port memory 14) shared among said plurality of data processors having a first port and a second port, and a global memory arbitration logic (bus controller 16) connected to said data processing core and said memory of each of said data processors (Fig. 1 and col. 2, lines 37-59), said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor and a far connection to said data processing core of additional data processors (col. 5, lines 5-14 wherein requests from multiple processing nodes 20 are recognized on the basis of position on the global bus 18, and thus for every processing node there are always close and far connections with respect the plurality of processing nodes), said global memory arbitration logic arbitrating access to said first port of said dual port memory among said data processing cores thereby providing a first type access (e.g. read type via buses 15 and 20) and arbitrating access to a second port of said dual port memory of another data processor among said data processing cores to said global memory arbitration logic of said another data processor thereby providing a second type access (e.g. write type via bus 18) (Figs. 1, 3, and col. 4, lines 39-65). However, Buktenica does not explicitly disclose granting a first type access to close data processing

cores and a second type access to far data processing cores. Hofmann teaches high priority device is granted a read request while the write bus may be granted to another lower priority device with higher priority write request (abstract and col. 3, lines 10-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement different priority levels for reads and writes as taught by Hofmann for the close and fare processing cores in the system of Buktenica wherein the first type access (read) is granted to a high priority processing core and a second type access (write) is granted to another processing cores to allow processing cores with high demand for reads and writes to have more frequent accesses to the memory and to allow reads and writes to remain operational by a low priority processing core when the higher priority processing cores requests the corresponding other bus operation (col. 3, lines 10-19).

As to claim 8, Buktenica further teaches each of said data processors further includes a peripheral bus (bus 18 and/or bus 20, bus 15) connected to said dual port memory for read and write access (Fig. 1), and Hofmann further teaches granting read access requests on said peripheral bus highest priority access to said first port and granting write access request on said peripheral bus highest priority access to said second port (col. 3, lines 10-19).

As to claim 9, Buktenica further teaches each of said data processors further includes a local memory (local memory 12) connected to said data processing core and directly accessible by said data processing core and not directly accessible by data processing cores of other data processors (Fig. 1).

As to claim 10, Buktenica further teaches said plurality of data processors consists of four data processors (Fig. 1 and col. 2, lines 30-36); said global memory arbitration logic of each data processor has a close connection to its corresponding data processor and another data processor and has a far connection to two other data processors (col. 5, lines 5-14 wherein requests from multiple processing nodes 20 are recognized on the basis of position on the global bus 18, and thus for every processing node there are always close and far connections with respect the plurality of processing nodes).

4. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buktenica et al. (5,669,009) (hereinafter Buktenica) in view of Hofmann et al. (6,513,089) (hereinafter Hofmann), and further in view of Lattimore et al. (5,956,286) (hereinafter Lattimore).

As to claim 3, the argument above for claim 2 applies. However, Buktenica does not explicitly disclose said first port of said dual port memory provides access to said dual port memory during a first portion of a repetitive time cycle; and said second port of said dual port memory provides access to said dual port memory during a second portion of said repetitive time cycle different from said first portion of said repetitive time cycle. Lattimore teaches a first port of a dual port memory provides read access to the dual port memory during a first portion of a repetitive time cycle; and a second port of the dual port memory provides write access to the dual port memory during a second portion of said repetitive time cycle different from said first portion of said repetitive time cycle (abstract and col. 4, lines 16-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide read operation from a first port

during a first portion of a repetitive time cycle and a write operation from a second port during a second portion of said repetitive time cycle as taught by Lattimore in the system of Buktenica and Hofmann to ensure that the multi port memory functions correctly (abstract).

As to claim 7, the argument above for claim 6 applies. However, Buktenica does not explicitly disclose said first port of said dual port memory provides access to said dual port memory during a first portion of a repetitive time cycle; and said second port of said dual port memory provides access to said dual port memory during a second portion of said repetitive time cycle different from said first portion of said repetitive time cycle. Lattimore teaches a first port of a dual port memory provides access to the dual port memory during a first portion of a repetitive time cycle; and a second port of the dual port memory provides access to the dual port memory during a second portion of said repetitive time cycle different from said first portion of said repetitive time cycle (abstract and col. 4, lines 16-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide read operation from a first port during a first portion of a repetitive time cycle and a write operation from a second port during a second portion of said repetitive time cycle as taught by Lattimore in the system of Buktenica and Hofmann to ensure that the multi port memory functions correctly (abstract).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses multi-port memory and/or shared memory accessing among a plurality of devices:

US Patent	6,487,643	Khare et al.
US Patent	5,960,458	Kametani
US Patent	6,480,927	Bauman
US Patent	5,761,455	King et al.
US Patent	6,545,935	Hsu et al.
US Patent	5,375,089	Lo
US Patent	6,604,174	Dean et al.
US Patent	6,625,686	Hasegawa et al.
US Patent	6,532,524	Fan et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
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PRIMARY EXAMINER